EXHIBIT 14

[redacted]

JEDEC Committee:

JC-40 Digital Logic

The products within JC-40's scope include digital integrated circuits without regard to their fabrication technology. The committee develops the definition of test parameters and their methods of measurement, and registration formats to promote standardization of type designations.

To accomplish these functions, the committee cooperates with other JEDEC committees and organizations on matters of terms and definitions, mechanical standardization, international standardization, and government liaison. The committee also maintains liaisons with user organizations to promote wide acceptance of the committee's output.

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Recent Documents

TS511X, TS521X Serial Bus Thermal Sensor Device Standard (/standards-documents/docs/jesd302-1a)	JESD302-1A	Aug 2023
SPD5118 HUB and SERIAL PRESENCE DETECT DEVICE STANDARD (/standards-documents/docs/jesd300-5b01)	JESD300-5B.01	May 2023
DDR5 Clock Driver Definition (DDR5CKD01) (/standards-documents/docs/jesd82-531a)	JESD82-531A	May 2023
PMIC50x0 Power Management IC Standard (/standards-documents/docs/jesd301-1a02-rev-185)	JESD301-1A.02 Rev. 1.8.5	Apr 2023

Definition of the SSTUB32869 Registered Buffer with Parity for DDR2 RDIMM Applications (/standards-documents/docs/jesd-82-27)	JESD82-27.01	Mar 2023
Fully Buffered DIMM Design for Test, Design for Validation (DFx) (/standards-documents/docs/jesd-82-28a)	JESD82-28A.01	Mar 2023
DEFINITION OF THE SSTVN16859 2.5-2.6 V 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR PC1600, PC2100, PC2700 AND PC3200 DDR DIMM APPLICATIONS (/standards-documents/docs/jesd-82-13a)	JESD82-13A.01	Mar 2023
DDR5 Registering Clock Driver Definition (DDR5RCD03) (/standards-documents/docs/jesd82-513)	JESD82-513	Feb 2023
DDR5 Registering Clock Driver Definition (DDR5RCD02) (/standards-documents/docs/jesd82-512)	JESD82-512	Feb 2023
DEFINITION OF THE SSTU32S869 AND SSTU32D869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS (/standards-documents/docs/jesd-82-12a)	JESD82-12A.01	Feb 2023

News

- Aug 2023
  JEDEC Board Presents 2023 Distinguished Executive Leadership Award to AMD CEO Dr. Lisa T. Su (/news/pressreleases/jedec-board-presents-2023-distinguished-executive-leadership-award-amd-ceo-dr)
- Apr 2022
  JEDEC to Host In-Person Memory Forum and DDR5 Workshop (/news/pressreleases/jedec-host-person-memory-forum-and-ddr5-workshop)
- Feb 2018
  JEDEC Events: Memory Tutorials, Mobile/IOT & Automotive Forums (/news/pressreleases/jedec-events-memory-tutorials-mobileiot-automotive-forums)

Subcommittees

JC-40.1: Digital Logic Families and Applications

JC-40.4: Registered & Fully Buffered Memory Support Logic
JC-40.5: Logic Validation and Verification
JC-40.7: Memory Support Logic for CXL

Join JC-40

Interested in JC-40's Digital Logic mission? Find out more about the benefits of JEDEC membership today.

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- New JEDEC Members (/join-jedec)
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Committee Meetings

Lisbon (/events-meetings/view_event/2462)	4 - 7 Mar 2024
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Montreal (/events-meetings/view_event/2062)	26 - 29 Aug 2024
Waikoloa (/events-meetings/view_event/2254)	2 - 5 Dec 2024

JEDEC Committee:

JC-42 Solid State Memories

The products within JC-42's scope include all memory integrated circuits and programmable logic devices, whether static or dynamic, without regard to their fabrication technology or application. Examples include large static and dynamic RAMs, ROMs, EEPROMs, and PLDs. Activities include the development of technical information and standards pertaining to pinouts, operational characteristics including reading and writing algorithms, test parameters, characterization, and registration formats. The committee maintains liaisons with other JEDEC committees and outside organizations to promote wide acceptance of the committee's actions.

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Recent Documents

STANDARD MANUFACTURERS IDENTIFICATION CODE (/standards-documents/docs/jep-106ab)	JEP106BI	Jan 2024
JC-42.6 MANUFACTURER IDENTIFICATION (ID) CODE FOR LOW POWER MEMORIES (/standards-documents/docs/jep166b)	JEP166E	Jul 2023
LOW POWER DOUBLE DATA RATE (LPDDR) 5/5X (/standards-documents/docs/jesd209-5c)	JESD209-5C	Jul 2023
Graphics Double Data Rate (GDDR6) SGRAM Standard (/standards-documents/docs/jesd250d)	JESD250D	May 2023

NAND Flash Interface Interoperability (/standards-documents/docs/jesd230c)	JESD230F.01	May 2023
Graphics Double Data (GDDR4) SGRAM Standard (/standards-documents/docs/sdram-3110508)	SDRAM3.11.5.8 R16.01	Mar 2023
GRAPHICS DOUBLE DATA RATE (GDDR5X) SGRAM STANDARD (/standards-documents/docs/jesd232a)	JESD232A.01	Mar 2023
GRAPHICS DOUBLE DATA RATE (GDDR5) SGRAM STANDARD (/standards-documents/docs/jesd212c)	JESD212C.01	Jan 2023
HIGH BANDWIDTH MEMORY (HBM3) DRAM (/standards-documents/docs/jesd238a)	JESD238A	Jan 2023
Secure Serial Flash Bus Transactions (/standards-documents/docs/jesd254)	JESD254	Dec 2022

News

- Aug 2023
  JEDEC Board Presents 2023 Distinguished Executive Leadership Award to AMD CEO Dr. Lisa T. Su (/news/pressreleases/jedec-board-presents-2023-distinguished-executive-leadership-award-amd-ceo-dr)
- Mar 2023
  JEDEC Creates New Automotive Steering Subcommittee (/news/pressreleases/jedec-creates-new-automotive-steering-subcommittee)
- Apr 2022
  JEDEC to Host In-Person Memory Forum and DDR5 Workshop (/news/pressreleases/jedec-host-person-memory-forum-and-ddr5-workshop)

More news (/committee-news/25)

Subcommittees

JC-42.1: Graphics RAMs (GDDRx)
JC-42.2: High Bandwidth Memory (HBM)
JC-42.3: Dynamic RAMs (DDRx)
JC-42.4: Non-Volatile Memory Devices

JC-42.5: Alternative Memory
JC-42.6: Low Power Memories
JC-42.9: Automotive Steering

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(/)

Global Standards for the Microelectronics Industry

JEDEC Committee:

JC-42.3 Dynamic RAMs (DDRx)

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Recent Documents

STANDARD MANUFACTURERS IDENTIFICATION CODE (/standards-documents/docs/jep-106ab)	JEP106BI	Jan 2024
Graphics Double Data (GDDR4) SGRAM Standard (/standards-documents/docs/sdram-3110508)	SDRAM3.11.5.8 R16.01	Mar 2023
GRAPHICS DOUBLE DATA RATE (GDDR5X) SGRAM STANDARD (/standards-documents/docs/jesd232a)	JESD232A.01	Mar 2023
184 Pin Unbuffered DDR SDRAM DIMM (/standards-documents/docs/module-40510)	MODULE4.5.10	May 2021
Annex A: Differences between JESD21C Release 29 and its predecessor JESD21C, Release 28. (/standards-documents/docs/annex-jesd21c)	AnnexA - JESD21C	Jan 2020
Dual Inline Memory Modules (DIMMs) Table of Contents (/standards-documents/docs/module-420toc)	MODULE4.20.TOC	Dec 2014
GDDR5 MEASUREMENT PROCEDURES (/standards-documents/docs/jep171)	JEP171	Aug 2014

Addendum No. 3 to JESD79-3, 3D STACKED SDRAM (/standards-documents/docs/jesd79-3-3-0)	JESD79-3-3	Dec 2013
Addendum No. 1 to JESD79-3 - 1.35 V DDR3L-800, DDR3L-1066, DDR3L-1333, DDR3L-1600, and DDR3L-1866 (/standards-documents/docs/jesd79-3-1a01)	JESD79-3-1A.01	May 2013
DDR3 SDRAM STANDARD (/standards-documents/docs/jesd-79-3d)	JESD79-3F	Jul 2012

JEDEC Committee:

JC-45 DRAM Modules

The scope of JC-45 is to develop standards for DRAM modules, cards, and socket interfaces. These standards are to address architectural, electrical, test, and SPD issues relating to memory design and manufacturing for commercial applications.

Memory module is defined as a single or multiple PCBs that predominantly include multiple memory, logic, and passive devices in a planar or 3D layout for use with sockets.

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Recent Documents

DDR5 Unbuffered Dual Inline Memory Module (UDIMM) Common Standard (/standards-documents/docs/jesd308a)	JESD308A	Jan 2024
JEDEC® Memory Module Label – for Compute Express Link® (CXL®) (/standards-documents/docs/jesd405-1a)	JESD405-1A	Jan 2024
DDR5 Clocked Unbuffered Dual Inline Memory Module (CUDIMM) Common Specification (/standards-documents/docs/jesd323)	JESD323	Jan 2024
DDR5 Clocked Small Outline Dual Inline Memory Module (CSODIMM) Common Specification (/standards-documents/docs/jesd324)	JESD324	Jan 2024

JEDEC Module Sideband Bus (SidebandBus) (/standards-documents/docs/jesd403-1c)	JESD403-1C	Dec 2023
Compression Attached Memory Module (CAMM2) Common Standard (/standards-documents/docs/jesd318-ver-102)	JESD318 Ver. 1.02	Nov 2023
DDR5 SERIAL PRESENCE DETECT (SPD) CONTENTS (/standards-documents/docs/jesd400-5b)	JESD400-5B	Oct 2023
DDR5 DIMM Labels (/standards-documents/docs/jesd401-5b)	JESD401-5B	Aug 2023
Annex K, Raw Card K, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM SODIMM Design Specification (/standards-documents/docs/module42025k01)	MODULE4.20.25.K.01	Aug 2023
DDR4 NVDIMM-N Design Standard (/standards-documents/docs/jesd248)	JESD248A.01	Apr 2023

News

- Dec 2023
  JEDEC Publishes New CAMM2 Memory Module Standard (/news/pressreleases/jedec-publishes-new-camm2-memory-module-standard)
- Aug 2023
  JEDEC Publishes New Standard to Support CXL Memory Module Implementation (/news/pressreleases/jedec-publishes-new-standard-support-cxl-memory-module-implementation)
- Aug 2023
  JEDEC Board Presents 2023 Distinguished Executive Leadership Award to AMD CEO Dr. Lisa T. Su (/news/pressreleases/jedec-board-presents-2023-distinguished-executive-leadership-award-amd-ceo-dr)

More news (/committee-news/26)

Subcommittees

JC-45.1: Registered DRAM Modules
JC-45.3: Unbuffered DRAM Modules

JC-45.4: Fully Buffered DRAM Modules
JC-45.5: Module Interconnect
JC-45.7: Memory Modules for CXL

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